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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,384	07/09/2003	Satoshi Machida	S004-5070	1248

7590 10/08/2004

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,384	MACHIDA, SATOSHI	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 8/11/04.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 7/19/2002. It is noted, however, that applicant has not filed a certified copy of the Japan 2002-210920 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 4-7 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplinsky (USP 5,164,612).

With respect to claims 4 and 9, Figure 2 of the Kaplinsky reference discloses a flip-flop, which includes: a data input terminal (D); a first switching element (15); a first inverter element (the inverter having an input connected to the output of 15 and an output connected to 17); a second switching element (17); a second inverter element (the inverter having an input connected to 17 and an output connected to Q); and signal generating means (19, 21) for generating first and second control signals (23, 25) for controlling the gates of the first and second switching elements (15, 17), respectively to simultaneously activate the first and second switching elements (controlling the select signals in 19 and 21 so that both of 19 and 21 outputs fixed signal H to

causes both 15 and 17 to turn on) to initializing the flip-flop and to alternately activate the first and second switching elements (controlling the select signals in 19 and 21 so that 19 outputs CLK/ and 21 outputs CLK) for activating the flip-flop circuit.

With respect to claims 5 and 10, Figure 2 of the Kaplinsky reference shows elements 15 and 17 are NMOS transistors.

With respect to claims 6 and 11, in Figure 2 of the Kaplinsky reference, the first MOS transistor is the PMOS transistor inside the first feedback CMOS inverter (i.e., the CMOS inverter having its output connected to the output of transistor 15, and its input connected to the input of transistor 17); and the second MOS transistor is the PMOS transistor inside the second feedback CMOS inverter (the CMOS inverter having its input connected to output Q, and its output connected to the output of transistor 17).

With respect to claims 7 and 12, Figure 2 of the Kaplinsky reference shows elements 15 and 17 are NMOS transistors.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaplinsky (USP 5,164,612) .

Note that Figure 2 of the Kaplinsky reference discloses a flip-flop as discussed above with regard to the rejection of claims 4-7 and 9-12 under 35 U.S.C. 102. The Kaplinsky

reference does not discloses a shift register. However, it is notoriously well-known in the art that a shift register can be made by connecting a plurality of D flip-flops in series (evidence can be seen from Figure 6 of Applicant's Admitted Prior Art). Therefore, it would have been obvious to one having skill in the art at the time of the invention to connect a plurality of D flip-flops of Figure 2 of Kaplinsky together for the purpose notoriously well-known of making a shift register. Thus, this modification forms a shift register comprising a plurality of flip-flops connected in series which meets all of the limitations of claims 8 and 13-16 because each of the plurality of flip-flops including a data input terminal (D), a first switching element (NMOS 15), a first inverter element (the inverter having an input connected to the output of 15 and an output connected to 17), a second switching element (NMOS 17), a second inverter element (the inverter having an input connected to 17 and an output connected to Q), signal generating means (19, 21) for generating first and second control signals (23, 25), a first MOS transistor (PMOS transistor inside the first feedback CMOS inverter, i.e., the CMOS inverter having its output connected to the output of transistor 15 and its input connected to the input of transistor 17), and a second MOS transistor (PMOS transistor inside the second feedback CMOS inverter, i.e., the CMOS inverter having its input connected to output Q and its output connected to the output of transistor 17) as discussed above with regard to the rejection of claims 4-7 and 9-12.

Response to Arguments

7. Applicant's arguments filed on 8/11/04 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 04, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816